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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/188,241	LUO, WENZHE	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 1998* is/are objected to by the Examiner.

11)☒ The proposed drawing correction filed on *14 June 2001* is: a)☐ approved b)☒ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Response to Amendment/Drawings

The amendment and proposed drawing changes submitted on Jun 14, 2001 have been reviewed and considered with the following results:

Although the proposed drawing corrections to Figs. 3, 5, 6A, 6B and 8 have been approved, and their respective drawing objections have been withdrawn, the proposed change to Fig. 2 is confusing. Why would power supply VDD now be indicated as "VDD-Vo"? Page 4, line 6 indicates a drain-source voltage of Vdd-Vo when switch MS is on. If "Vo" is a voltage across load CL (e.g. see Fig. 4), then the drain-source voltage of switch MS would not be VDD-Vo because of the voltage drop across transistor MC. Therefore, the proposed drawing change to Fig. 2 has been disapproved, and Fig. 2's drawing objection has been maintained with respect to what the applicant considers "Vo". The modified objection is described later under the appropriate section.

The new abstract is approved, and the objection to the abstract has been withdrawn.

The amended claims and/or comments have overcome the rejections of claims 3, 4, 10, 11 and 18 under 35 U.S.C. 112, second paragraph. Therefore, those rejections have been withdrawn. However, the rejections under 35 U.S.C. 112 for claims 15-17, and 20-22 have been maintained. For example, it appears the rejection of claim 20 on page 6 of the previous Office Action was not even addressed. Therefore, those remaining rejections are described later under the appropriate section, and comments

with respect to the applicant's arguments/comments are described under the Response to Arguments section.

None of the prior art rejections, either under 35 U.S.C. 102(e) or under 35 U.S.C. 103(a), described in the previous Office Action have been withdrawn. All of those rejections are repeated, with minor modifications to correct inadvertent oversights and/or improve some word flow, later under the appropriate section. Comments with respect to the applicant's arguments/comments are described later under the Response to Arguments section.

It is also noted a new objection to the disclosure is described later. This objection was found when the disclosure was reviewed in an attempt to get a better understanding of what the applicant is trying to claim.

Drawings

The drawings remain objected to because Fig. 4 does not show "Vo", which is described on page 4, line 6, and the applicant's proposed drawing change to Fig. 2 adds confusion with respect to what the applicant considers "Vo." Therefore, correction is still required for Fig. 2.

Specification

The disclosure is objected to because of the following informality: it is now believed "load side of the switch MC" on line 18 of page 7 should be --load side of the switch MS--. An appropriate correction is required.

Claim Rejections under 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 15-17, and 20-22 remain rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 15 has a current sink and a current source (from claim 2). However, it is not clear how the current sink and current source relate to the load. For example, the applicant's Fig. 7 shows a current sink 720, and a current source 740, wherein Fig. 8 shows current source 740 is capacitor CL. Therefore, what the applicant considers the load within claims 15-17 is not understood with respect to the recited current source, because it appears none of the applicant's circuits show the sink, source, and load all within one circuit. Related to this confusion, it is not clear in claim 20 how "a load" relates to the current source/ charged capacitor. Isn't the load the charged capacitor? The description "continuously receives said current flowing from said current source" in claims 21 (lines 8-9) and 22 (lines 9-10) is still considered misleading. For example, the applicant's Fig. 5 shows current IA from current source 420 will flow to load 440 only when transistor switch 430 is conducting. However, when transistor switch 430 is open, current IA cannot flow from the current source to the load.

Dependent claims carry over the rejection(s) from claim(s) upon which they depend.

Claim Rejections under 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-5, 8-10, 12, and 18-22 remain rejected under 35 U.S.C. 102(e) as being anticipated by Ravon. For the following descriptions, Figs. 2-4 of Ravon will be considered and/or referred to, wherein one of ordinary skill in the art would be able to recognize the relationships between the figures. In Fig. 2, Ravon shows a current source switching circuit comprising a transistor switch M1; what can be deemed a pull-down mirror path M2,13,14 in parallel with transistor switch M1 (e.g. they are both coupled between terminal E and ground); and first load C'. Current source 11 (see column 3, line 31) is shown in detail in Fig. 3 (see column 4, lines 44-45). Fig. 4 shows first load C', transistor M2, and details of comparator 14. Although transistor switch M1 is replaced by diode D1 in Fig. 4 (see column 6, lines 16-18), Ravon also discloses a transistor provides better efficiency on column 6, lines 24-25. Therefore, for the following description, diode D1 of Fig. 4 will be replaced with a transistor switch (e.g. M1 of Fig. 2) for improved efficiency, wherein block 13 of Fig. 2 will be used to control the on/off operations of both transistors M1 and M2. One of ordinary skill in the art would recognize that current source 11 (shown in Figs. 2 and 3) provides current I to terminal E of Fig. 4. Although the reference does not clearly disclose the "substantially continuously" reduction of "charge injection" as recited within the claims, one of ordinary skill in the art would know it relates to the current received by the load capacitor. When transistor M2 is off and transistor switch M1 is on, first load C' receives current I (from

current source 11) through transistor switch M1 (e.g. see Fig. 2). Besides charging first load C', the current also charges capacitor C1 through resistor R1 (see Fig. 4). [Note that the structure of first load C', capacitor C1, resistor R1, and amplifier 20 closely corresponds to the respective load 440, capacitor C1, resistor R1, and amplifier 400 structure of the applicant's Fig. 5.] When transistor switch M1 is turned off, and transistor M2 is turned on, capacitor C1 will help maintain the voltage across first load C' (i.e. between terminal S and ground), and less current will be required to completely charge first load C' back up once transistor switch M1 is turned back on. Therefore, transistor switch M1 and pull-down mirror path M2,13,14 substantially continuously reduce the charge injection into first load C', and claim 1 is anticipated. Fig. 2 clearly shows current source 11 connected between power source Vc and a first side (i.e. terminal E) of transistor switch M1, and first load C' connected between ground and a second side (i.e. terminal S) of transistor switch M1, thus anticipating claims 2 and 3. Since first load C' is a charging capacitor, and transistor M1 is a MOS transistor, claims 4 and 5 are also anticipated. Transistor M2 of the pull-down mirror path M2,13,14 can be deemed a pull-down amplifier, anticipating claim 8. When transistor M2 is conducting, its output (i.e. drain) follows the current source 11 side of the transistor switch M1 by allowing the current to flow through transistor M2, thus claim 9 is anticipated. Transistors M1 and M2 receive their respective signals from control 13 (see Fig. 2) which allows transistor M2 to be turned off, and then transistor M1 to be turned on (see column 4, lines 28-30). Therefore, transistor M2 is deemed a complementary pull-down mirror path transistor switch which operates opposite the transistor switch M1,

anticipating claim 10. Since current source 11 comprises MOS transistor M3, claim 12 is anticipated. Transistor/switch M2 provides a pull-down mirror path parallel with current switch M1, wherein switches M2 and M1 are substantially turned on and off alternatively, anticipating 18 and 19 because when transistor M1 is off, the capacitor C1 will basically maintain a voltage on load capacitor C', thus substantially continuously reducing the charge injection flowing to the load. Current source 11 comprises a charged capacitor C (see Fig. 3), thus anticipating claim 20. Transistor switch M1 connects current source 11 to load C', and it is substantially simultaneously turned off when switch M2 is turned on. When switch M2 is on, the current I from current source 11 flows through the pull-down mirror path M2,13,14. Since capacitor C1, of the pull-down mirror path M2,13,14, helps maintain a voltage across load C', the charge injection will be reduced when transistor switch M1 is opened, and claim 21 is anticipated. The upper output of block 13 is coupled to the gate of transistor switch M1 and is deemed the means for opening transistor switch M1, and the lower output of block 13 is coupled to the gate of switch M2 and is deemed the means for closing switch M2, wherein current I from current source 11 flows through the pull-down mirror path M2,13,14. Since capacitor C1, of the pull-down mirror path M2,13,14, helps maintain a voltage across load C', the charge injection will be reduced when transistor switch M1 is opened, and claim 22 is anticipated.

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 7 and 11 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Ravon as applied to respective claims 1 and 10 above, and further in view of the applicant's Prior Art Fig. 3. As described previously, the basic current source switching circuit is shown and disclosed by the reference of Ravon. However, the reference does not show or disclose the use of the serial combinations of transistors as recited within claims 6, 7 and 11. Ravon shows only a single transistor for transistor switch M1 and for complementary pull-down mirror path transistor switch M2. It would have been obvious to one of ordinary skill in the art to replace each of transistors M1 and M2 of Ravon's circuit with a respective compensated transistor switch of the applicant's Fig. 3. Transistors 302b, 304b and 306b would correspond to the first serial combination of respective first compensating, functional MOS, and second compensating transistors, wherein transistors 302a, 304a and 306a would correspond to the second serial combination of respective first complementary compensating, complementary functional MOS, and second complementary compensating transistors, thus rendering obvious claims 6, 7 and 11. As the applicant admits on page 3, lines 8-28, the use of such compensated switches are conventional/well known means for reducing charge injection. Since Ravon's circuit can be considered a current type switch circuit for charging first load C', the compensated switch of the applicant's Fig. 3 would help reduce charge injection even more within the circuit if that was desired.

Claims 13-17 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Ravon as applied to claim 1 above. As described previously, Figs. 2 and 4 of

Ravon show a circuit with a transistor switch M1, pull-down mirror path M2,13,14, current source 11, and first load C'. However, the reference does not clearly show or disclose a pull-up amplifier as recited within claim 13. It would have been obvious to one of ordinary skill in the art to modify the circuitry of Ravon by reversing the polarities (i.e. Vc and ground would be reversed) and transistor types. The reversal of the polarities and transistor types would provide a means for a higher output voltage (e.g. closer to power source Vc). The reversal would replace all the MOS transistors (i.e. M1-M6) with their complementary transistors (i.e. an NMOS transistor would be replaced with a PMOS transistor). In this case, transistor M2 would be coupled between power source Vc and the common connection of current source 11/transistor switch M1, and first load C' would be coupled between power source Vc and terminal S. Therefore, transistor M2 could be deemed a pull-up amplifier, rendering claim 13 obvious. Current source 11 would be coupled between ground and one side (i.e. terminal E) of transistor switch M1, rendering obvious claim 14. Since current source 11 would be sinking current to ground, it could be deemed a current sink coupled between ground and one side (i.e. terminal E) of transistor switch M1, rendering claims 15 and 16 obvious. The circuit would comprise charging capacitor C', coupled between power source Vc and one side (i.e. terminal S) of transistor/current switch M1, rendering claim 17 obvious.

Claims 1-5, 8-10, 12, 18 and 19 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Harston. In Fig. 3 Harston shows a current source switching circuit comprising transistor switch MP2; a pull-down mirror path MP3 in parallel with said transistor switch MP2; and first load 10pf. Although the reference does not clearly disclose a reduction in charge injection, it would be obvious to one of ordinary skill in the art that resistor 37.5Ω would reduce the charge injection flowing to first load 10pf because it will start discharging first load 10pf when transistor switch MP2 is turned off.

Therefore, as long as transistor switch MP2 is off, and there is a charge on first load 10pf, the charge injection flowing to the first load will be substantially continuously reduced, thus rendering claim 1 obvious. [MP3 is considered a pull-down mirror path since it mirrors the operation of the transistor switch MP2 and allows the current from transistor MP1 to flow down to ground. See column 2, lines 64-68.] Fig. 3 also shows a current source MP1 (a MOS transistor) coupled between power source CURRENT CELL and the first side of transistor switch MP2; and load 10pf is a charging capacitor 10pf coupled between ground and a second side of transistor switch MP2, thus rendering obvious claims 2-5. Since a transistor can be deemed an amplifier, pull-down mirror path MP3 can be deemed a pull-down amplifier, rendering claim 8 obvious. When transistor MP3 is conducting, its output (i.e. drain) follows the current source MP1 side of the transistor switch MP2 by allowing the current to flow through transistor MP3, thus rendering obvious claim 9. Transistors MP2 and MP3 receive their respective signals DATAB and DATA. Therefore, transistor MP3 can be deemed a complementary pull-down mirror path transistor switch operating the opposite of transistor switch MP2, rendering claim 10 obvious. It is complementary since it receives a control signal which is a complement of the signal received by transistor switch MP2. Since current source MP1 is a MOS transistor, claim 12 is rendered obvious. Transistor/switch MP3 provides a pull-down mirror path parallel with current switch MP2, wherein switches MP3 and MP2 are alternatively on and off, rendering obvious claims 18 and 19 because when transistor MP2 is off, the resistor 37.5Ω will discharge load 10pf, thus substantially continuously reducing the charge injection flowing to the load.

Claims 6, 7, and 11 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Harston as applied to claims 1 and 10 above, and further in view of the compensated transistor switch of the applicant's Prior Art Fig. 3. Harston shows

only a single transistor for each of transistor switch MP2 and complementary pull-down mirror path transistor switch MP3. It would have been obvious to one of ordinary skill in the art to replace each of the single transistors MP2 and MP3 of Harston's circuit with a respective compensated transistor switch of the applicant's Fig. 3. Transistors 302b, 304b and 306b would correspond to the first serial combination of respective first compensating, functional MOS, and second compensating transistors, wherein transistors 302a, 304a and 306a would correspond to the second serial combination of respective first complementary compensating, complementary functional MOS, and second complementary compensating transistors, thus rendering obvious claims 6, 7 and 11. As the applicant admits on page 3, lines 8-28, the use of such compensated switches are conventional/well known means for reducing charge injection of switches in analog circuits. Since Harston's circuit in Fig. 3 can be considered a current switch circuit related to an analog circuit, the compensated switch of Fig. 3 would help reduce charge injection within the circuit if that was desired.

Claims 13-17 and 20 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Harston as applied to respective claims 1 and 18 above. As described previously, Fig. 3 of Harston shows a circuit with a transistor switch MP2 (30), pull-down mirror path MP3 (32), current source MP1 (20), and load capacitor 10pf. However, the reference does not clearly show or disclose a pull-up amplifier as recited within claim 13. It would have been obvious to one of ordinary skill in the art to modify the circuit of Fig. 3 by reversing the polarities and transistor types. The reversal of the polarities and transistor types would provide a means for a higher output voltage. The reversal would replace all the PMOS transistors (i.e. MP1, MP2 and MP3) with NMOS transistors. In this case transistor 32 would be coupled between power source CURRENT CELL and the common connection of current source 20 and transistor

switch 30. Therefore, transistor 32 could be deemed a pull-up amplifier, rendering claim 13 obvious. Current source 20 would be coupled between ground and one side of transistor switch 30, rendering obvious claim 14. Since current source 20 would be sinking current to ground, it could be deemed a current sink coupled between ground and one side of transistor switch 30, rendering claims 15 and 16 obvious. The circuit would comprise charging capacitor 10pF, coupled between power source CURRENT CELL and one side of transistor/ current switch 30, rendering claim 17 obvious. Deeming capacitor 10pF a current source, claim 20 is rendered obvious. It would charge up to CURRENT CELL when transistor 32 conducts, and discharge (or supply current) when transistor 30 conducts.

No claim is allowable as presently written.

Response to Arguments

The applicant's arguments filed Jun 14, 2001 have been fully considered but they are not persuasive. The applicant argues: 1) the claims are clear as written; 2) the current is continuously received by the load when the transistor switch is open; 3) Ravon fails to teach the switch/path that provides a reduced charge injection to the load; 4) that "charge injection is **NOT** simply current required to charge a load capacitor"; 5) Ravon and the AAPA fail to teach a switch/path that provides reduced charge injection; 6) Harston fails to teach the switch/path that provides a reduced charge injection to the load; 7) the references do not show/disclose a mirror path since "current does NOT flow to the output substantially continuously; 8) Harston and the AAPA fail to teach a switch/path that provides reduced charge injection; 9) the claims clearly claim the current flows from the source to the load; 10) its unclear why the terms are un-clearly

recited; and 11) the examiner is ignoring two of the most relevant limitations within the claims.

1-2) The applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. The arguments/comments with respect to claim 15 basically describes the claim's chain of dependency and the limitations claimed. However, the arguments/comments do not address the rejection under 35 U.S.C. 112 with respect to what the applicant actually considers the load since the recited claim also has a current source and current sink. Since it doesn't appear that any of the applicant's circuits clearly show all three (i.e. source, sink, and load) within the same circuit, the examiner requests the applicant to point out in the figures and/or specification a circuit comprising current source, current sink and load, with all those separate elements identified by reference character. This way, the examiner will have a better understanding of what the applicant is actually trying to claim that has actually been shown or disclosed. The arguments with respect to claims 21 and 22 merely indicate the claims must be read as a whole, and that they are clear. As with claim 15 above, these arguments/comments do not address the rejections under 35 U.S.C. 112. Even after considering the claim limitations and the applicant's figures, clarification is still required which clearly explains how current from the current source can still flow to the load when the switching transistor is open as recited within the claims. For example, the explanation can use

the elements of the applicant's Fig. 5 circuit to clarify the claims' recited limitations. Also, see the related current flow discussion in "9)" described later.

3-4) The applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. For example, the applicant argues that Ravon fails to teach a transistor switch and pull-down mirror path that reduces charge injection flowing to a load. However, Ravon's transistor M1 is a transistor switch; and M2,13,14 is a pull-down mirror path because it will allow current I to be pulled down (i.e. flow) to ground when transistor M2 is on, and M2 is clearly coupled in parallel with respect to transistor M1 (and C'). As for the reduced charge injection, the reference does not specifically disclose that terminology. However, Ravon clearly discloses the invention limits transient variations related to "abrupt variations" of current (see column 2, lines 2-8) and that "circuit 11 generates, permanently, a current I" (see column 4, lines 63-65). Since this implies current source 11 is never turned off, terminal E will not charge up to the voltage level of power source Vc because of the associated voltage drop across M1 or M2. Therefore, the drain-source voltage across transistor M1 will be substantially constant (due to the charges on load C' and the capacitor C1 within path M2,13,14, and the voltage on terminal E that results from the current I flowing either through M1 or M2). When transistor M1 is either turned on or off, there will not be a surge of current due to the small drain-source voltage difference. By minimizing this type of current

surge, Ravon's circuit does "substantially continuously" reduce charge injection to the load.

5) Although it is true the AAPA (e.g. applicant's admitted prior art) does not teach the switch/path by itself, the combination of Ravon and AAPA does relate current variations (one type of charge injection) with a switch and path. The applicant admits on pages 3-4 of the disclosure that the AAPA relates to "Another conventional technique to reduce charge injection in a current switch circuit." Since the circuit of Ravon limits variations of voltage/current, and the AAPA is a known means for reducing charge injection (e.g. one type of current variation), it would be obvious to one of ordinary skill in the art to use the switch of the AAPA as the switch in Ravon's circuit, thus providing a switch/path with reduced charge rejection.

6) The applicant argues that Harston fails to teach the switch/path that provides a reduced charge injection to the load. However, one of ordinary skill would recognize transistor 30 of Harston is a transistor switch; and transistor 32 is a pull-down mirror path since it pulls down the current from current source 20 by allowing it to flow to ground when transistor is conducting, and because of the complementary input signals DATAB/DATA to transistors 30/32, their operation will be mirrored (e.g. one will be off while the other is on - see column 2, lines 64-68). Since either transistor 30 or 32 is always on, allowing the current from transistor 20 to continuously flow, the voltage on the common node between transistor 20 and transistors 30/32 will be substantially constant because it will not be pulled up to power source CURRENT CELL. Therefore, when transistor 30 is turned on, the drain-source voltage difference of transistor 30 will

be less than if no current would flow through current source 20, and the common node reached the voltage level of power source CURRENT CELL. Thus, the circuit of Harston does provide "substantially continuous" reduced charge injection to the load during operation.

7) The applicant also argues that the references do not show/disclose a mirror path since current does NOT flow to the output/load continuously. However, that limitation in itself is questionable with respect to the rejections under 35 U.S.C. 112 described earlier. For example, it is still not known how the applicant's own Fig. 5 circuit can provide the current IA from current source 420 to the load 440 when transistor switch 430 is open. Once switch 430 is open, current IA must flow to pull-down mirror path 450. However, there is no clear understanding how current IA can flow through amplifier 400 (which is believed to be an op amp), then through resistor R1, and finally to load 440. Although there may be a related current flow between load 440 and capacitor C1 within pull-down mirror path 450, that current is not current IA from current source 420. If the applicant means current IA from current source 420 is continuously flowing, then both Ravon and Harston show/disclose a continuous current flow from their respective current sources. Ravon's current I from current source 11 is continuous (i.e. permanent – see column 4, lines 63-64) because of the current paths related to transistors M1 and M2, wherein Harston's current from current source 20 will flow continuously due to the complementary operation of transistors 30 and 32. Therefore, until it is clear what the applicant means by continuous flow of the current from the

current source to the load, those limitations are believed to be met by the circuit operation of both Ravon and Harston.

8) The applicant's argument with respect to Harston and the AAPA is similar to that addressed in "5)" above. Using the same type of reasoning, the use of the conventional switch of the AAPA as the switch within Harston's circuit would be obvious to one of ordinary skill in the art.

9) The applicant's argument with respect to current flowing to the load when the transistor switch is open fails to comply with 37 CFR 1.111(b) because it amounts to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references because it is believed the applicant's own circuits/disclosure do not clearly show/disclose the limitation as recited and presently understood. Page 12 of the applicant's amendment/arguments indicate the current from the current source flows through the pull-down mirror path (an alternate current path), and page 8, lines 2-7 of the disclosure supports that basic interpretation. However, the examiner disagrees with the applicant's comments that the "Applicant discloses a pull-down mirror path in the disclosure as an alternate path for current to flow through to reach the load" as described on page 12 of the amendment. This is because the arguments and disclosure fail to clearly point out how the current flowing through the pull-down mirror path actually flows to the load. For example, it is believed amplifier 400 (shown in the applicant's Fig. 5) is an operational amplifier. Therefore, it is not understood how a current will flow into the inverting input – and out of the non-inverting input + of the

applicant's amplifier 400 to the load. It is believed current IA will flow through transistor MT, and then down to ground through undisclosed circuitry within amplifier 400. However, one of ordinary skill in the art would recognize that when current IA flows through switch 430, both load capacitor CL and capacitor C1 will become charged. Once switch 430 is opened, the charges between capacitors CL and C1 will balance out after some initial current flow across resistor R1 to account for the capacitors' voltage difference due to the voltage drop across resistor R1. Since load 440 will maintain a fairly constant voltage, due to the voltage on charged capacitor C1, there will not be a large change in voltage/current when transistor switch 430 is either opened or closed. When switch 430 is closed, current IA is coupled to load 440.) This in itself will reduce charge injection to the load. However, the current associated with resistor R1 and capacitor C1 is not the current from the current source as the claims clearly recite. Therefore, the current flowing to the load after the switch opens, as recited within some claims, is questionable and clarification is required. [It is noted that the examiner does not equate ground to the load. The examiner maintains the cited references show an alternative current path for the current from the current source to flow when the transistor is open. This will help maintain a constant current flow from the current source, even when the transistor switch is open.]

10) The applicant does not understand why the examiner believes the recited terms are unclear, and states (on page 13) that "the Examiner is not reviewing the claimed limitation of a mirror path which is clearly claimed within the claims", and "the Examiner is not considering the claimed limitations." The examiner has been

attempting to understand what the applicant has disclosed, recited, and shown. However, the claims, disclosure and/or previous comments/arguments made by the applicant have not clearly disclosed, or clarified, the problems identified by the examiner. Therefore, understanding some of the claimed limitations is difficult. According to MPEP 2111, the claims must be "given the broadest reasonable interpretation consistent with the specification." Therefore, both Ravon and Harston show circuitry which provide an alternative path for the current from the current source to flow through. That alternative path related circuitry has been deemed a pull-down mirror path, which the examiner has clearly provided reasoning for, as previously described. With respect to charge injection, the examiner believes that has also been clearly described within the Office Actions. For example, when transistor switch M1 of Ravon is opened, the charge stored across load C' at terminal S, will be held substantially constant by resistor R1 and capacitor C1 of the mirror path 14. Also, since Ravon discloses current I is permanent, it would be understood than the voltage at terminal E would be substantially constant due to current I flowing through M2. Therefore, whether transistor switch M1 turns on or off, there will be no large voltage/current change at terminal S, and from this, one of ordinary skill in the art would understand that charge injection is reduced (with respect to if a large change would occur). Even if, for some reason, there might be a larger change (e.g. spike) in voltage/current when the transistor switch M1 is turned on or off, the parallel combination of resistor R1/capacitor C1 across load capacitor C' would help absorb the change, thus also reducing charge injection to the load. This reduction occurs when the

transistor switch is turned on or off, or whenever a variation of voltage/current is occurs at terminal S. Therefore, the examiner is not simply considering charge injection as current flowing to the load. Since the applicant's disclosure, figures, and arguments/ comments have not satisfactorily clarified how the current from the current source would still flow to the load once the transistor switch is open, the examiner believes the references of Ravon and Harston continue to read on the claim limitations.

11) The applicant also states "the Examiner is ignoring two of the most relevant limitations within the claims, a reduction of **charge injection** and a **mirror path**." This comment relates to various arguments/comments described previously. However, another explanation will be described here. The examiner has not ignored the limitations, and has taken a lot of time trying to understand the claimed invention, and then explain and/or clarify how the prior art references meet those limitations. MPEP 2111 states "The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach." Therefore, the examiner believes one of ordinary skill in the art would understand the circuits shown and disclosed within each of the references of Ravon and Harston can be interpreted as having a reduction in "charge injection" and a "mirror path" as described by the examiner. It appears the applicant is not satisfied with the reasoning described by the examiner; fails to help clarify sections specifically identified by the examiner; and would probably only accept a reference that uses the same terminology as the applicant's application.

Under these circumstances, the rejections described above, and in previous Office Actions, are still considered proper.

THIS ACTION IS MADE FINAL. The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for this Art Unit is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE

Terry L. Englund
22 August 2001

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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